Epitaxy-on-Electronics:

Monolithic Integration of Heterostructure Devices on Commercially-Processed Gallium Arsenide Integrated Circuits

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Workshop on Advanced Spacecraft Technologies
Pasadena, California
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OUTLINE

The incentives for optoelectronic integration

OEIC technologies
- hybrid
- monolithic

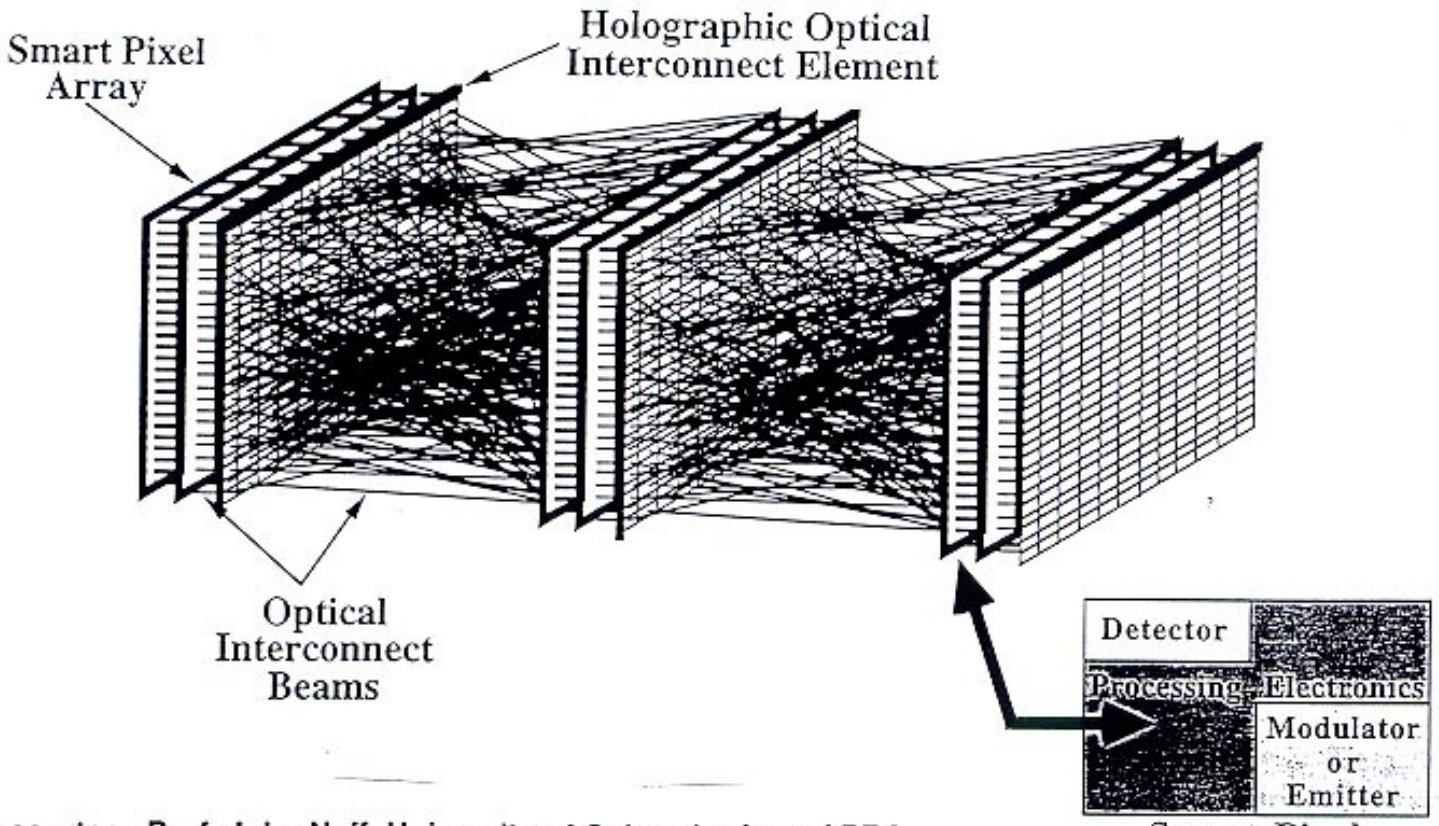
The epitaxy-on-electronics technique
- concept and process flow
- constraints and solutions
- monolithic emitters
- state of the art

The OPTOCHIP project
- project overview
- participants
- design examples
- current status

Summary
- accomplishments
- the future

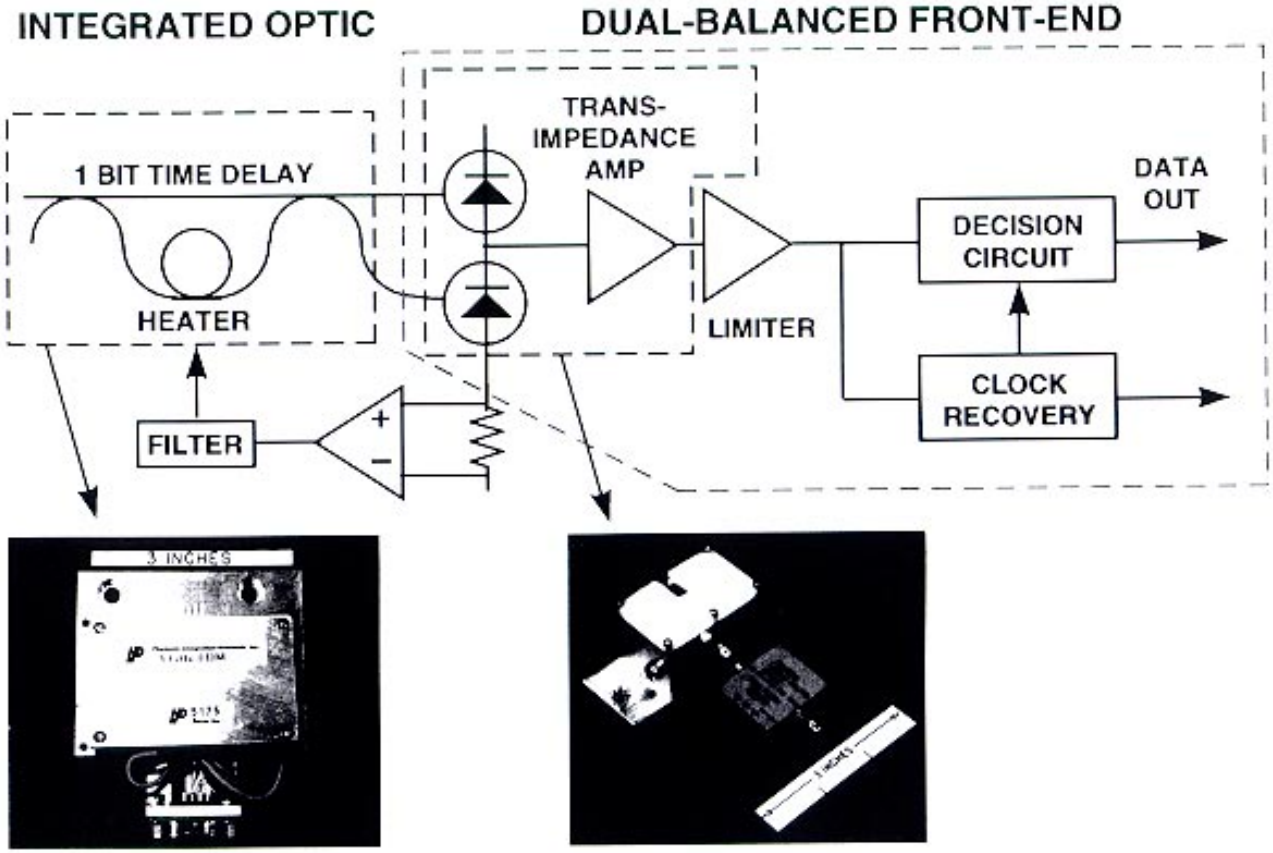
GLOBAL INTERCONNECTION

Free-Space Interconnection Enables a Broader Range of Interconnect Topologies



Vugraph courtesy Prof. John Neff, University of Colorado; from APRA Ultra-Photonics II Workshop, November, 1995

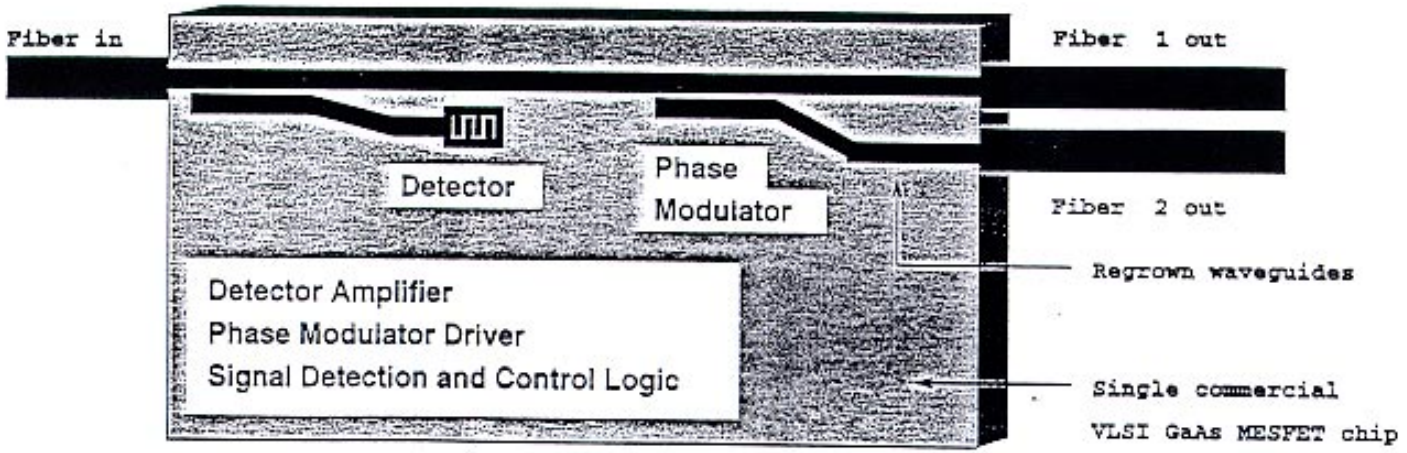
OPTICAL DPSK DEMODULATOR



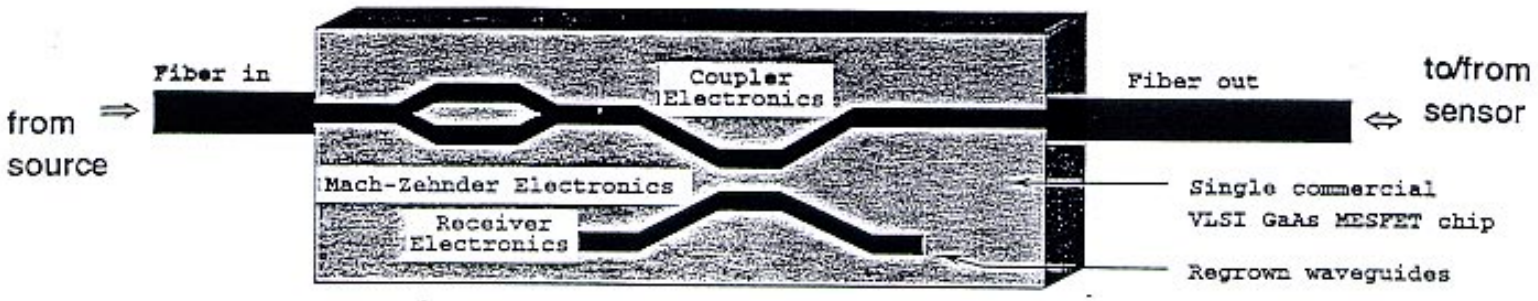
- ELECTRICAL BANDWIDTH REQUIRED ~ DATA RATE
- INTEGRATED-OPTIC COMMERCIALLY AVAILABLE
- INTEGRATED FRONT END REQUIRES DEVELOPMENT

277279-2P

INTEGRATED OPTICS (fiber-coupled) OEICs



Network Packet Router



Transmit/Receive Module

Approaches to

OPTOELECTRONIC INTEGRATION

- * **Hybrid**

  - discrete optoelectronic devices bonded to processed VLSI chips and/or MCMs

  - a short term solution at best, with serious density, power, cost, and speed limitations

* **Stacked Heterostructure Technologies (Epi-fIrst)**

  - multi-layer heterostructures: layers for different devices grown seequentially creating "stack"

  - current approaches require development of the entire technology

* **Epitaxy on VLSI (Epitaxy-on-Electronics)**

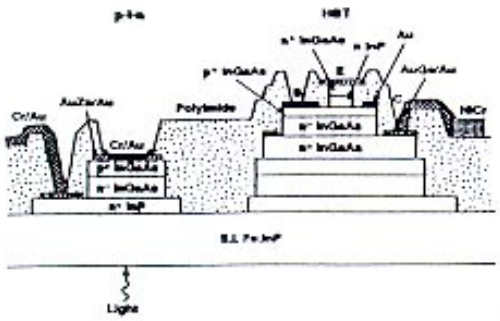
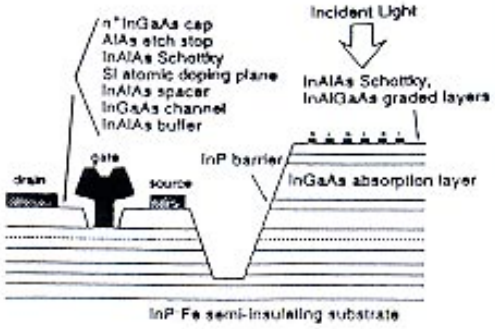
  - optoelectronics grown on completed electronics

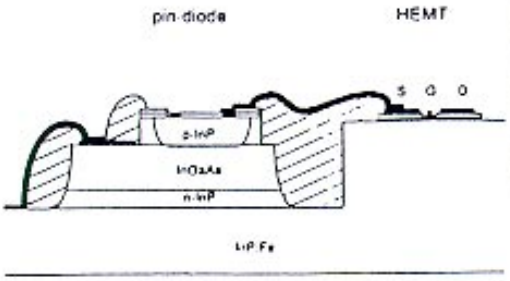
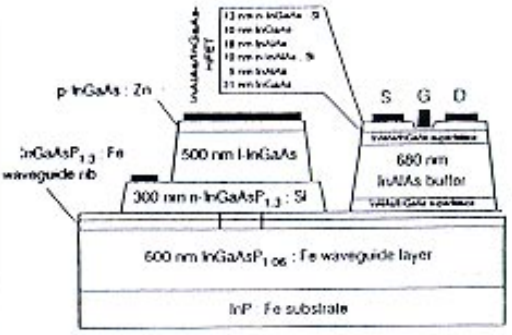
  - builds on exisiting VLSI base; compatibility is the key issue

  - examples: GaAs-on-Si

    GaAs-on-GaAs

EPITAXY FIRST

pin-HBT	MSM-HFET
	
Single MOMBE run	Single MOVPE run
A_E= 3 x 8 μm^2; β= 65	L_G= 0.2 μm; g_m= 800 mS/mm
f_T= 70 GHz	f_T= 105 GHz

pin-HFET	WGPD-HFET
	
Two-step MOVPE	Two-step MOVPE+MBE
L_G= 1.0 μm; g_m= 300 mS/mm	L_G= 0.2 μm; g_m = 800mS/mm
f_T= 30 GHz	f_T= 37 GHz

from L. M. Lunardi, "InP-based Monolithically Integrated Photodetectors," Paper TuF1 at International Conference on Indium Phosphide and Related Materials, May 1997

The MIT/NCIPT OEIC Process

"EPI-on-ELECTRONICS"

GaAs wafers

↓

Commercial
GaAs IC Process

↓ Electronics complete

Epitaxy

↓ Heterostructrures added

Photonic Device
Processing

Final Interconnection

Packaging

↓ OEIC processing complete

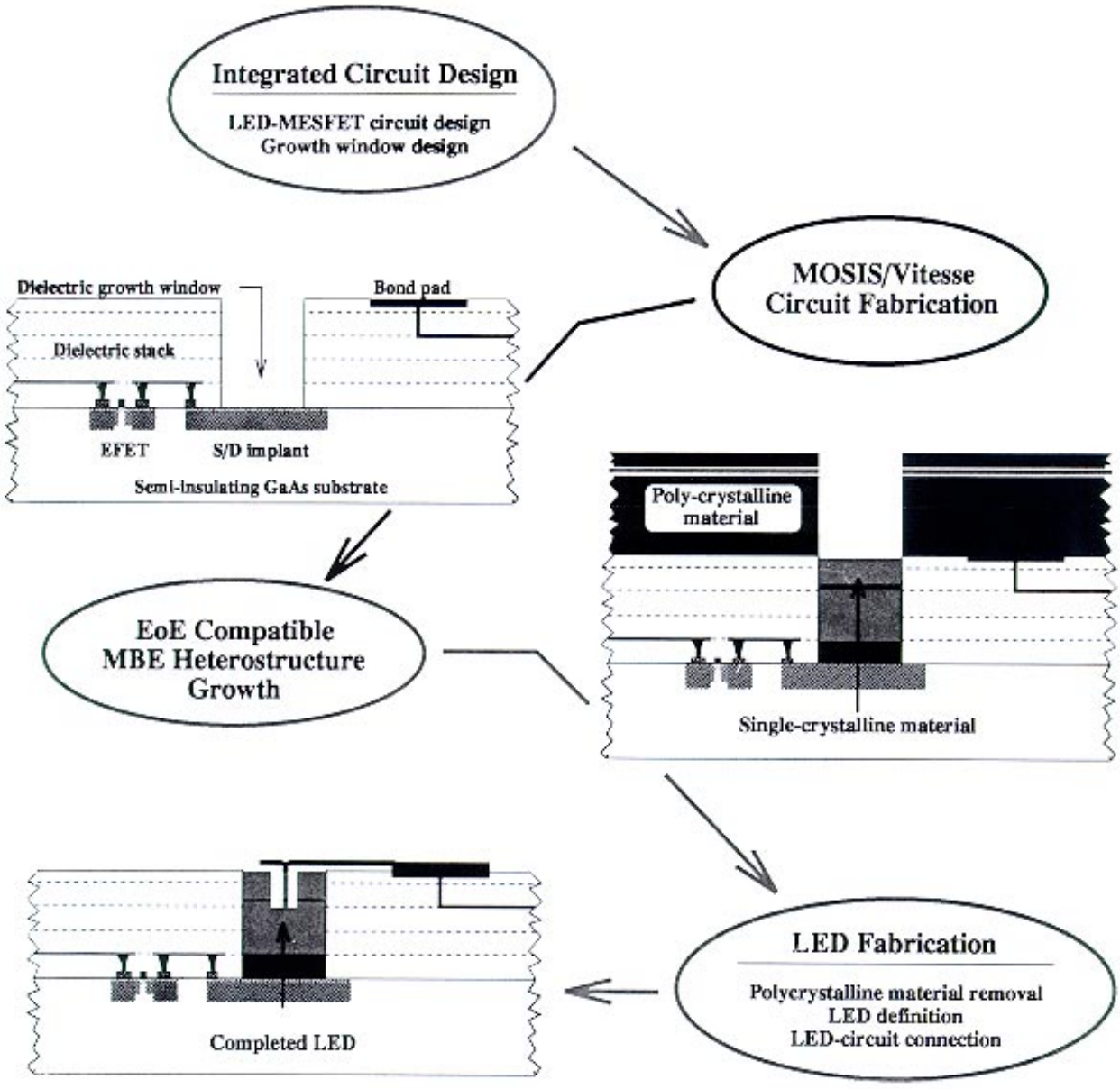
Monolithic OEICs
to Users

- our uniqueness and underlying tenet:

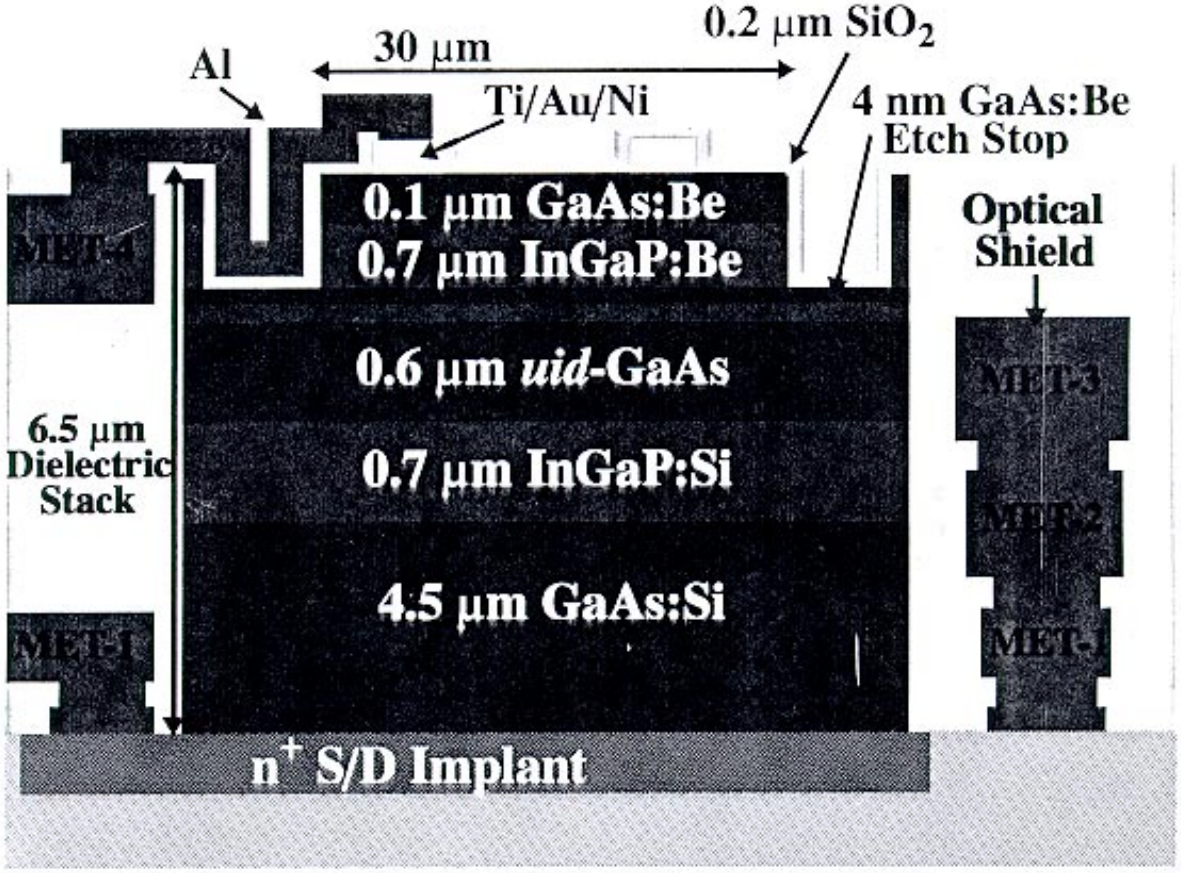
“Build on the existing commercial GaAs VLSI technology base”

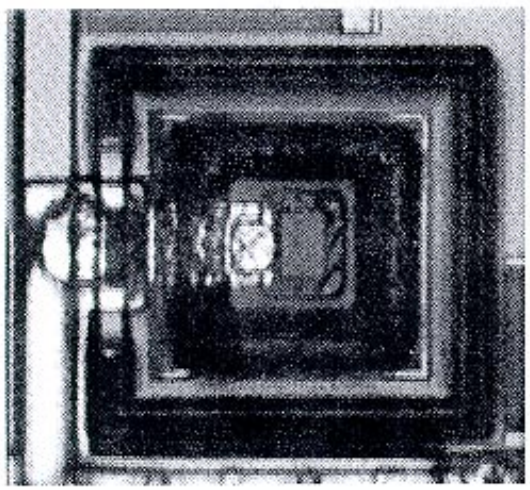
Epitaxy-On-Electronics Technique

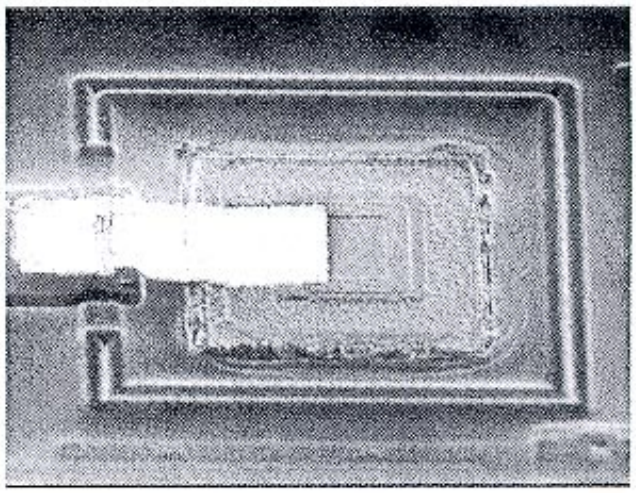
Process Flow



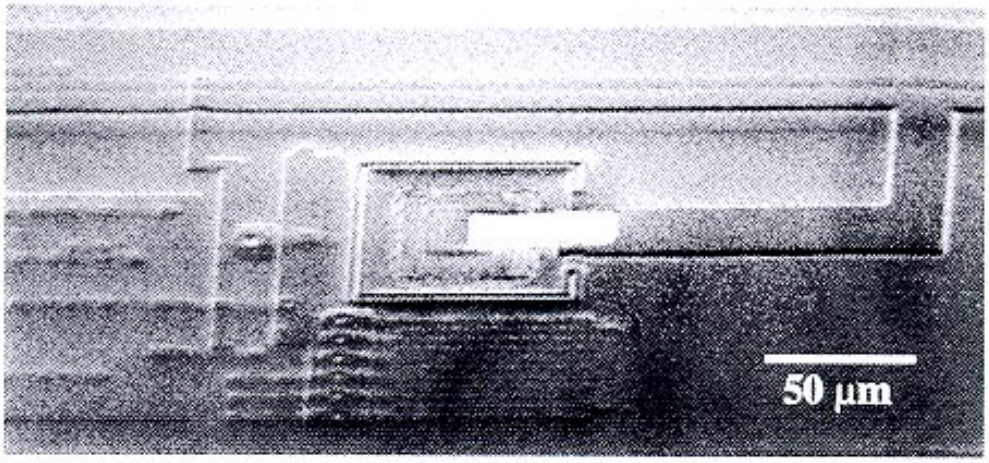
Integrated GaAs/InGaP LED

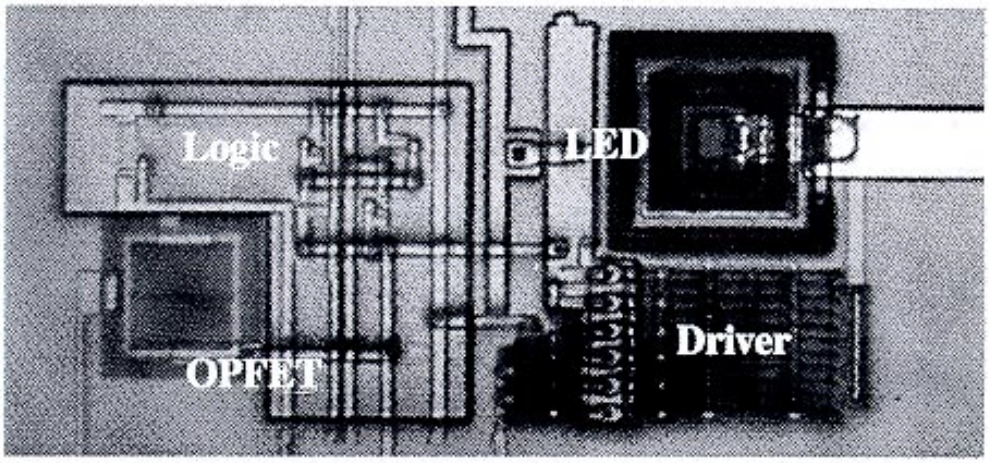


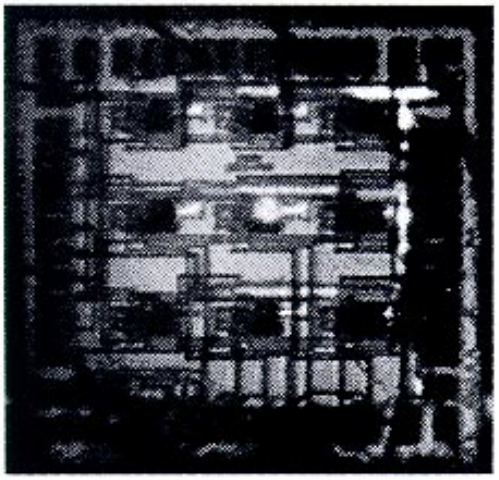


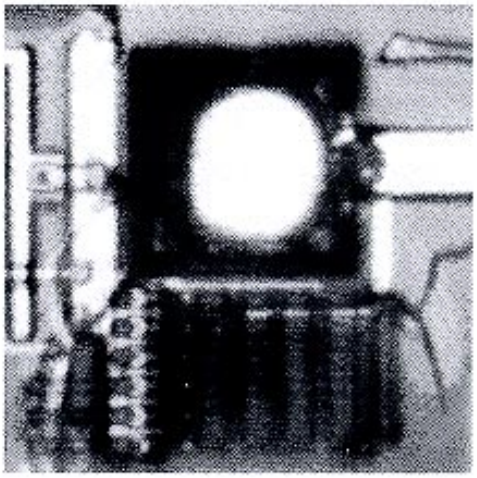


Integrated LED and Driver

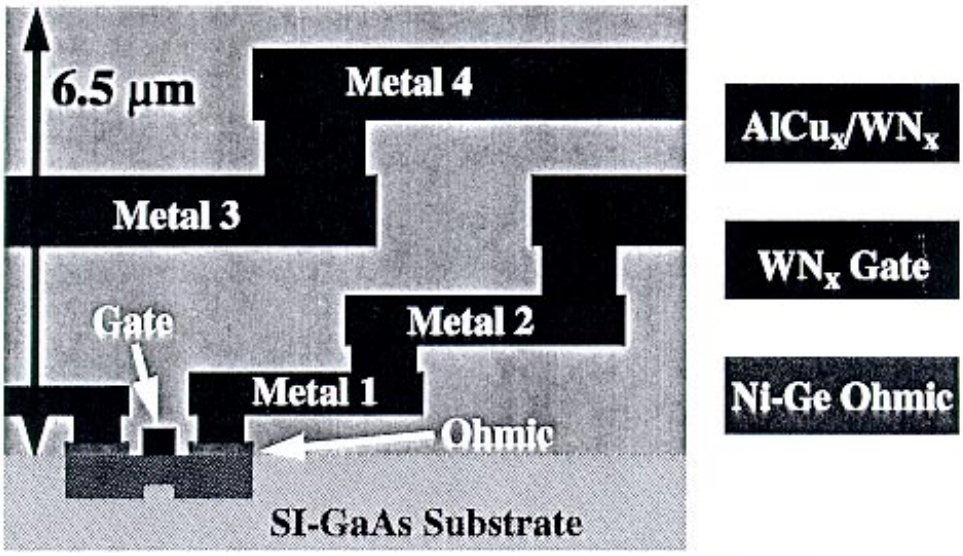


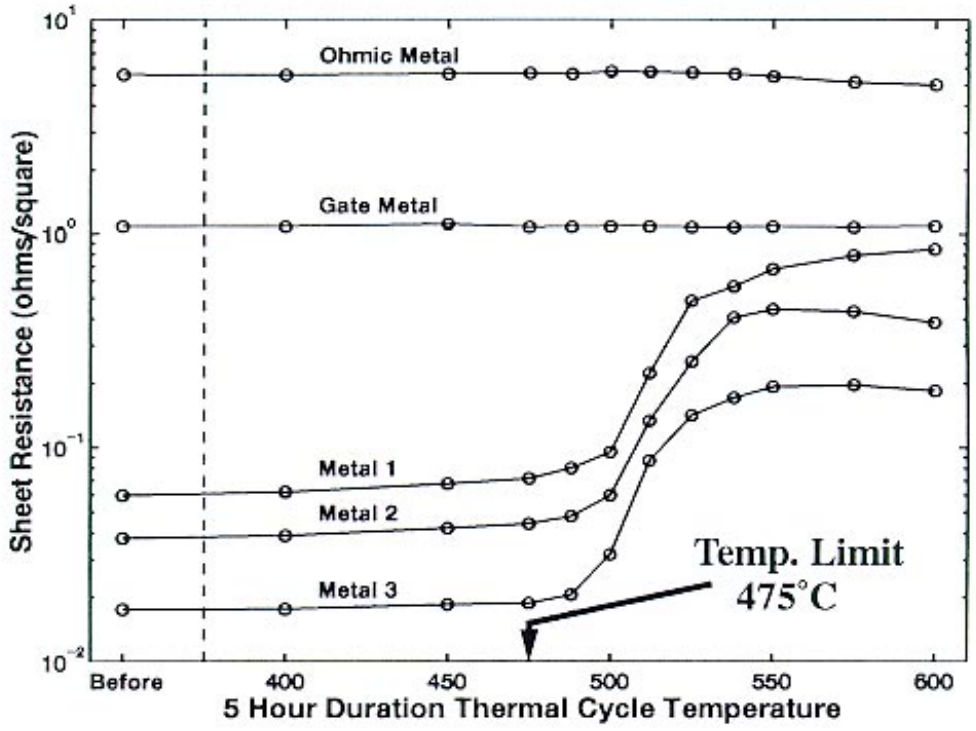






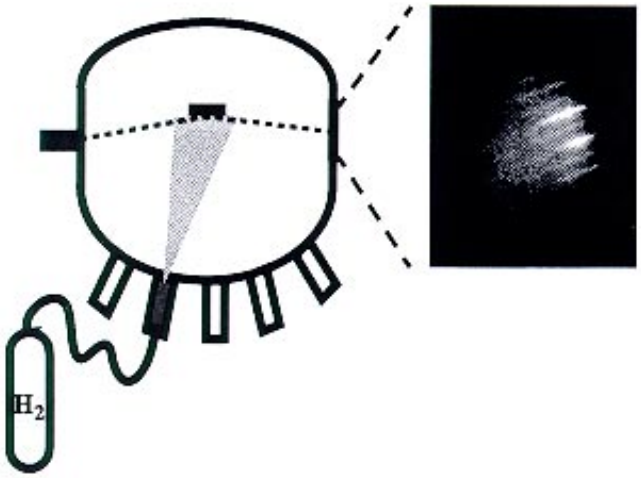
Thermal Stability
of Commercial GaAs VLSI





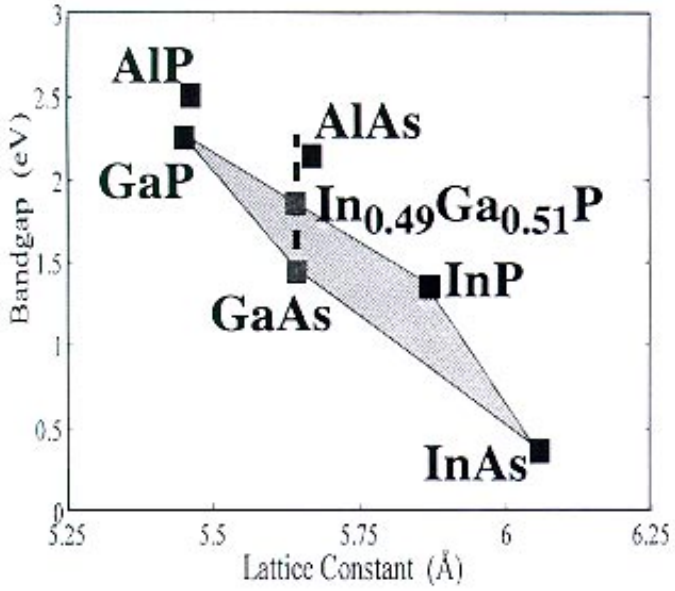
Sub-475°C MBE

Low-temperature native oxide removal:



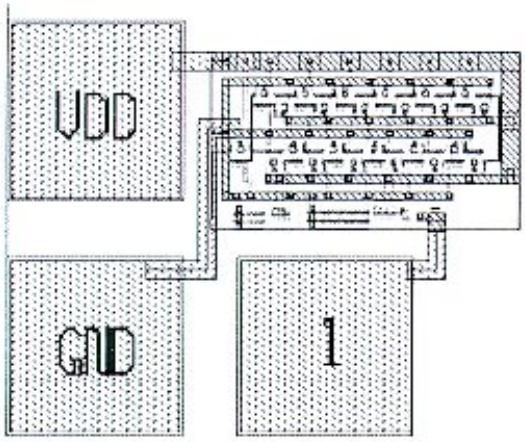
- **Conventional MBE:** desorb GaAs-oxide at 580°C
- **Cracked atomic hydrogen removes GaAs-oxide with T_{sub}< 470°C**

InGaAsP/GaAs:

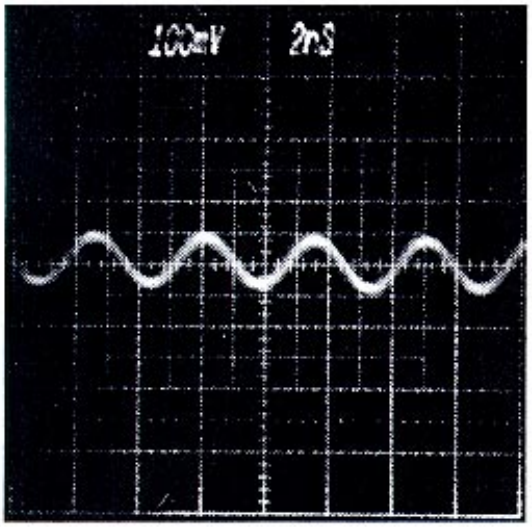


- AlGaAs best grown above 600°C
- **InGaAsP/GaAs growth is EoE-compatible**
- **InGaAs/GaAs/InGaP QW-SCH laser grown entirely at 470°C: J_{th}=200 A/cm^2**

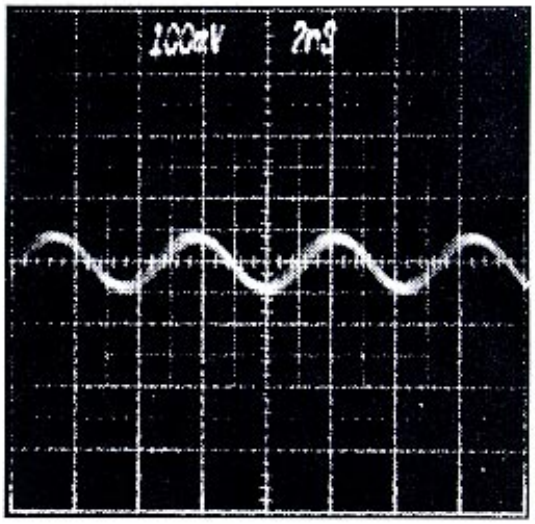
EoE Electronics
on OPTOCHIP-1



- 23-stage DCFL ring-oscillator determines gate delay
- Before growth: t_p = 76.1 ps
- After growth: t_p = 89.1 ps



Before Growth



After Growth

Epitaxy-on-Electronics OEIC Technology Development

Monolithic OEICs by epitaxy on commercial GaAs VLSI custom ICs (must stay below 475°C)

Recent Highlights

- In-situ atomic hydrogen cleaning under 470°C (eliminates 580°C oxide desorption step)

- Low threshold lasers grown at 470•C (material suitable for VCSELs and IPSELs)

- Monolithic integration of InGaP-based LEDs (far superior to previous LEDs using AlGaAs)

- Close interaction with IC foundry through MOSIS (improved custom layout and special handling)

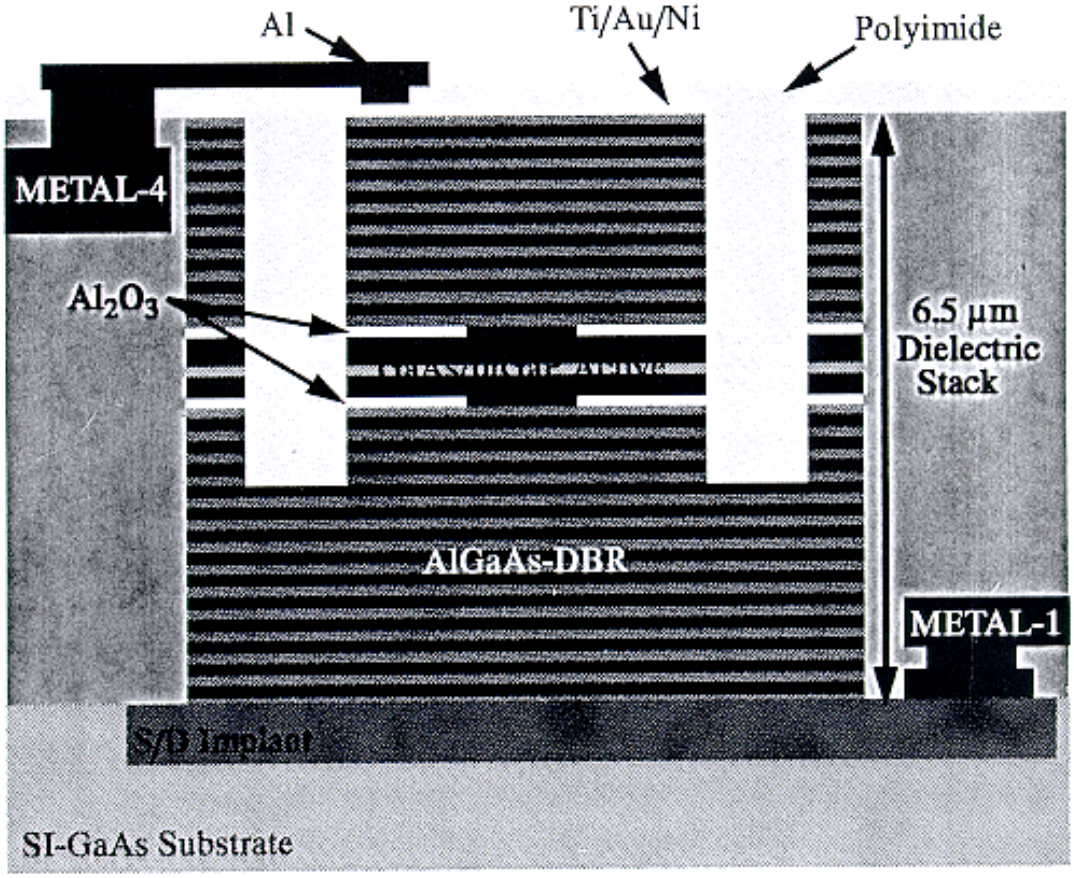
- Extensive OEIC CAD tools and systems developed (multi-project OEICs; OPTOCHIP offerings)

Immediate Objectives

- Monolithic integration of VCSELs and IPSELs

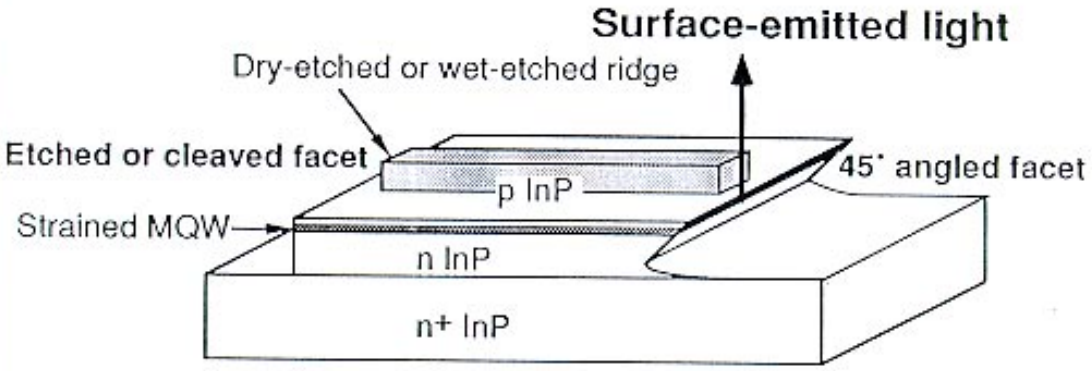
- Additional research foundry offerings

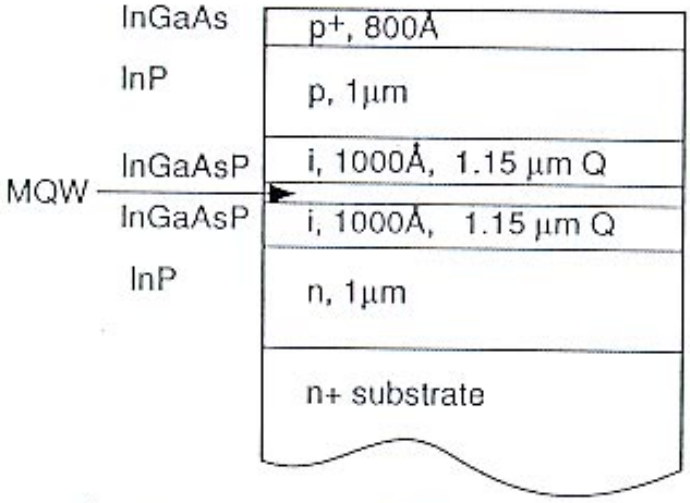
Integrated VCSEL
(projected)



- **Patterned after:**
  Lear *et. al.*, Elect. Lett., Vol. 32, 1996, pp. 457-458.
- **Features:**
  Top or bottom emission
  Efficient current/field confinement (double oxide aperture)
  Embedded in dielectric
  Heat sunk through substrate
  Low parasitics (>20 GHz demonstrated at Sandia)
  Simple 4-mask process

Etched-facet FCSEL

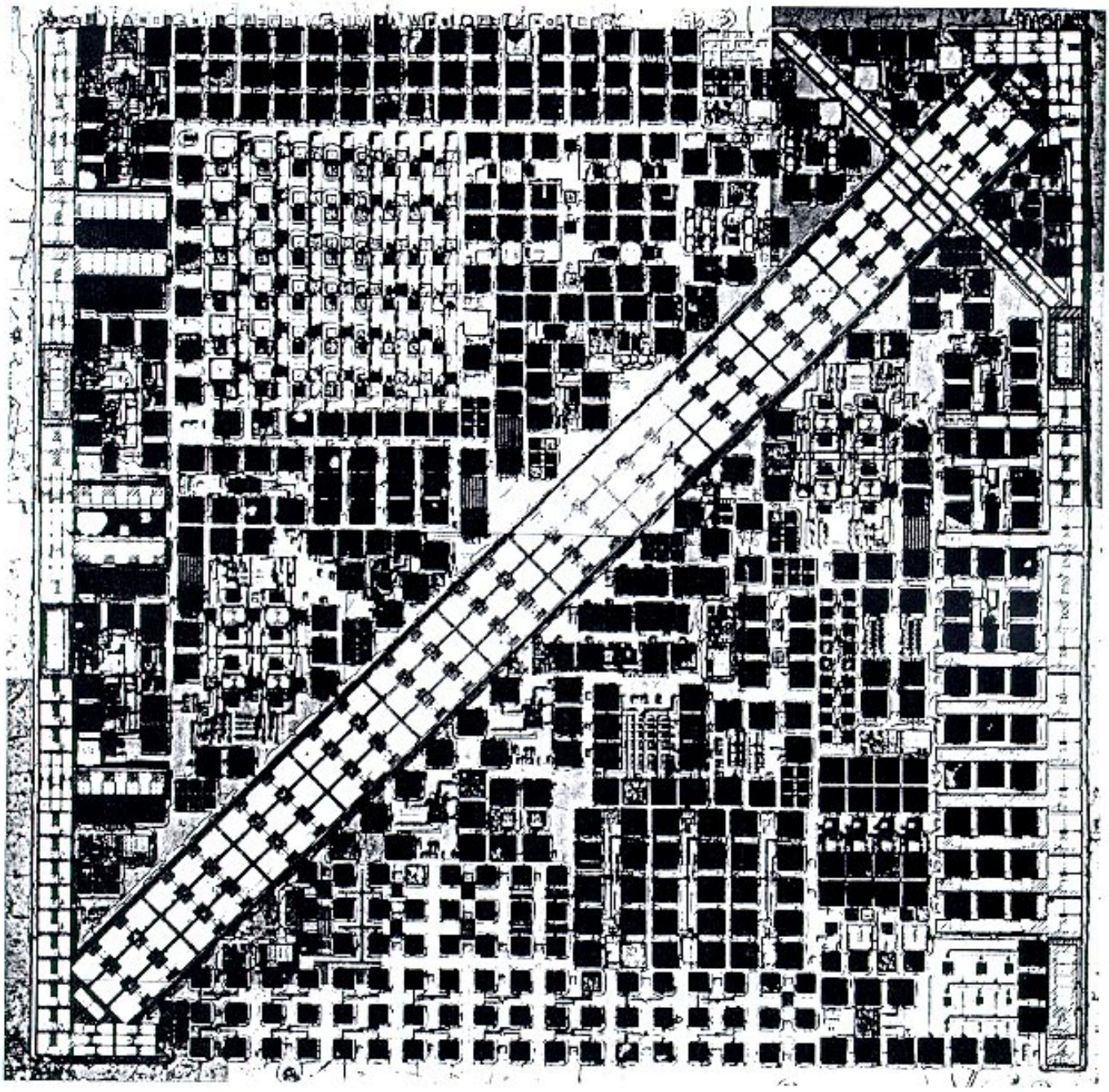




- Grown by gas-source MBE.
- Strained InGaAsP MQW :
  - 60Å wide well with λ_g = 1.4 μm
  - 105Å wide barrier with λ_g = 1.15 μm
  - ~ 0.8% compressive strain
- Internal loss : 10 cm^{-1}, internal efficiency : 70%

Courtesy Prof. Steve Forrest, Princeton University

Processed MIT OEIC-3 Chip



Contains integrated resonant tunneling diodes (RTDs)

The OPTOCHIP Project:
A prototype OEIC foundry

Objectives:

- To make the epitaxy-on-electronics OEIC technology available to the broader user community

- To stimulate applications of OEICs and motivate further development of the epitaxy-on-electronics technology

Overview:

- Participating groups design and receive 2 mm square OEIC chips

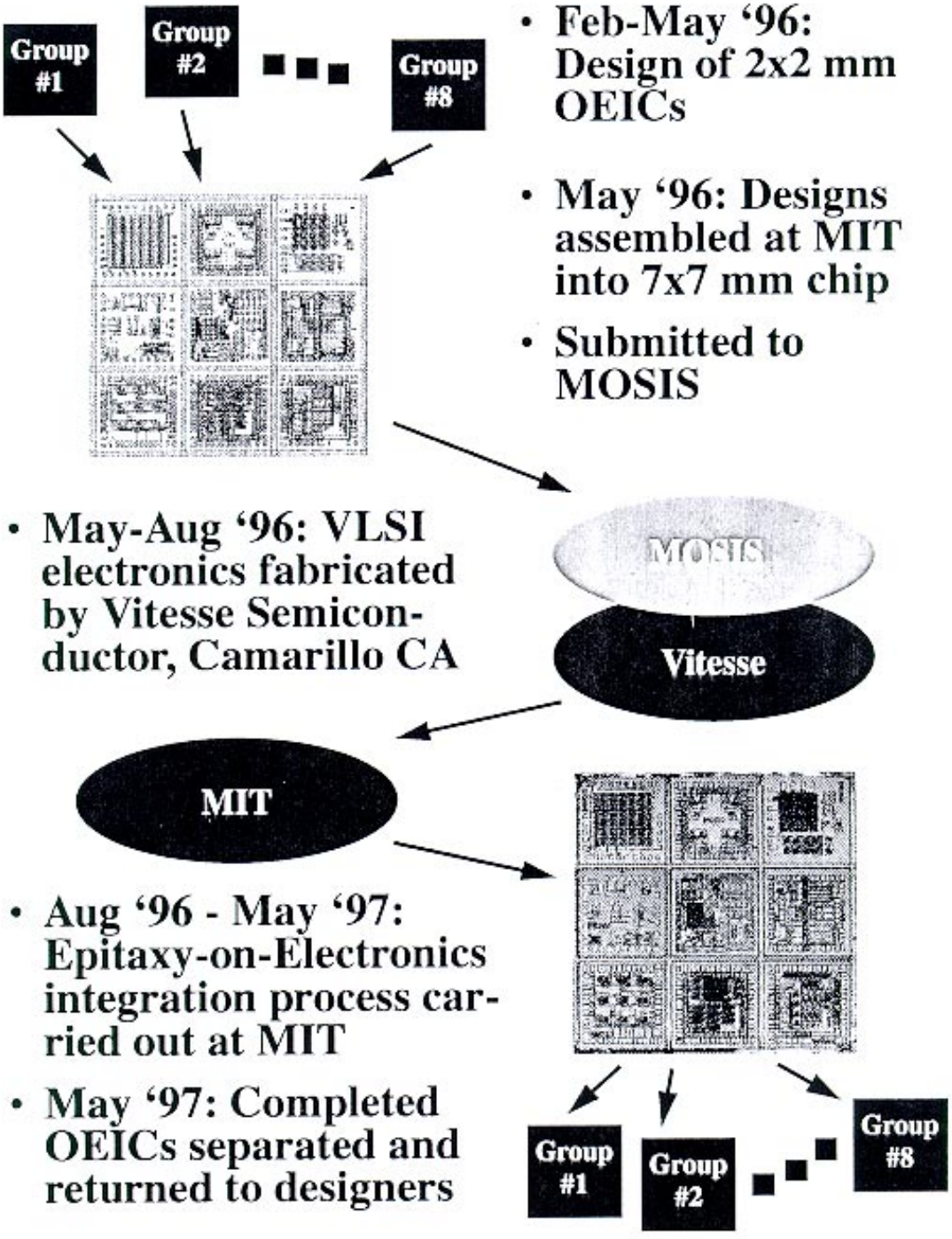
- The chips contain LEDs and photodetectors (msm detectors and/or OPFETs) monolithically integrated with GaAs enhancement- and depletion-mode MESFETs

- Design support provided by NCIPT researchers at MIT and USC. A standard optical bond pad library supplements existing FET design files.

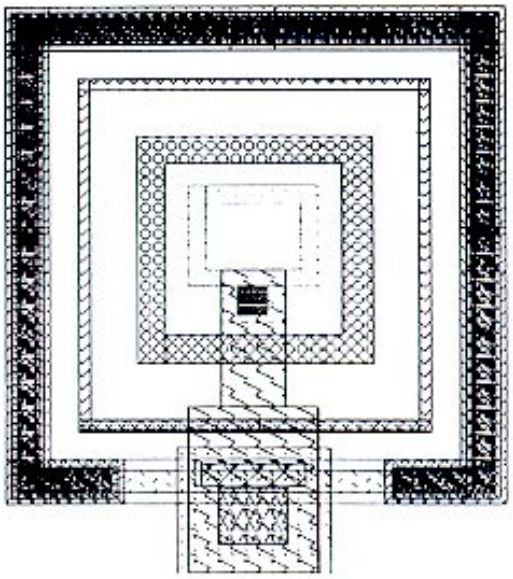
- Pre-growth preparation, epitaxy, and post-epitaxy processing done at MIT using facilities of Profs. Fonstad and Prof. Kolodziejski, and the Microsystems Technology Lab

- The first foundry offering cycle has been completed and chips were sent to the participating groups in early May '97

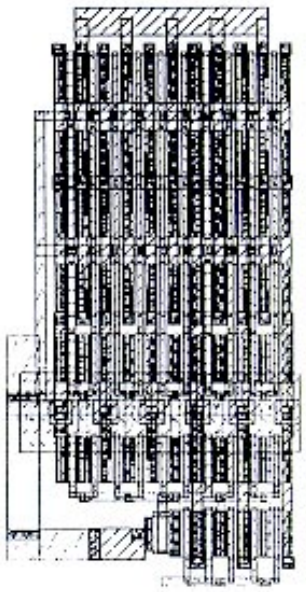
The OPTOCHIP Project



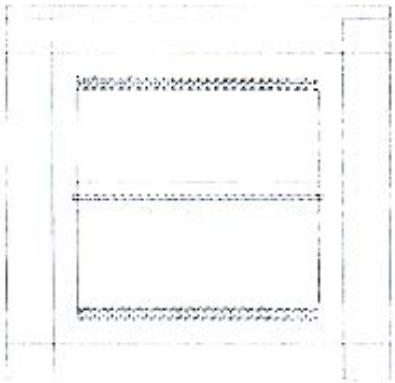
Drop-in Cells
on OPTOCHIP-1



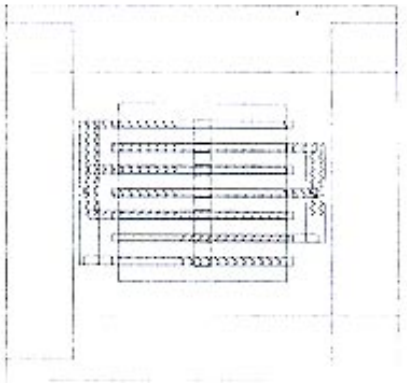
LED



Driver

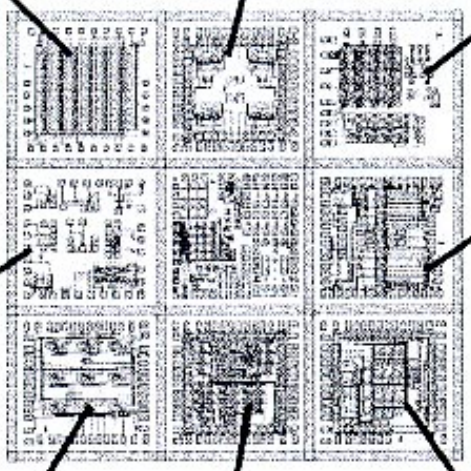


OPFET Photodetector



MSM Photodetector

OPTOCHIP-1



Free-space Interconnect Prototype
George Mason

Neural Array
Caltech

Connectionist Correlation Network
Colorado State

Dynamic Smart Pixels
McGill

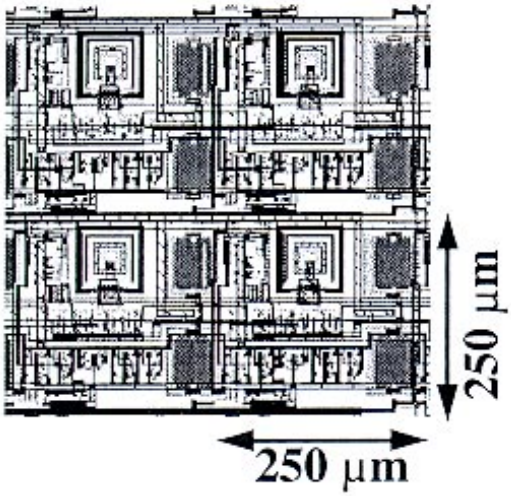
Multiplicative Lateral Inhibition Neural Network
U. of Washington

Error Diffusion Neural Network
West Point

Remote Sensor Interface
TCU

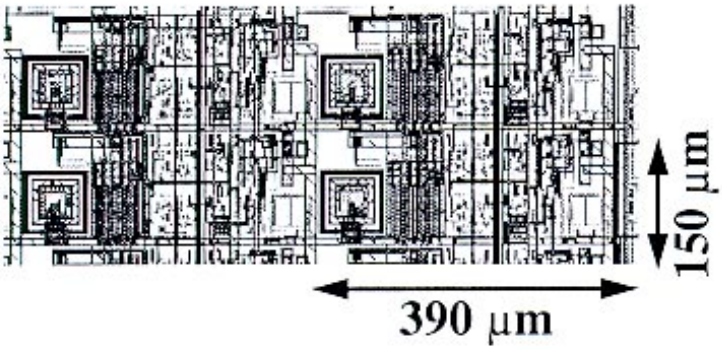
Multi-channel Network Interface
&
Smart Pixel Parallel Data Processor
USC

Smart Pixels
on OPTOCHIP-1



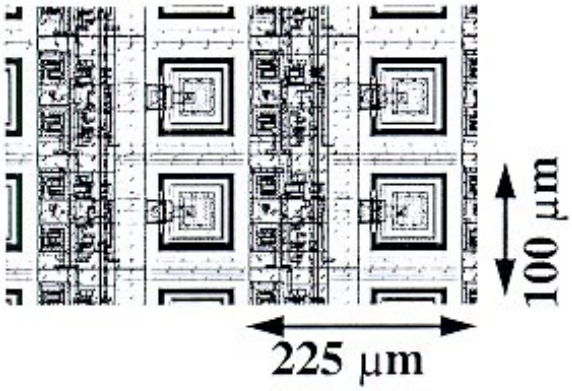
CSU:

- **1600 Pixels/cm^2**



USC:

- **1709 Pixels/cm^2**

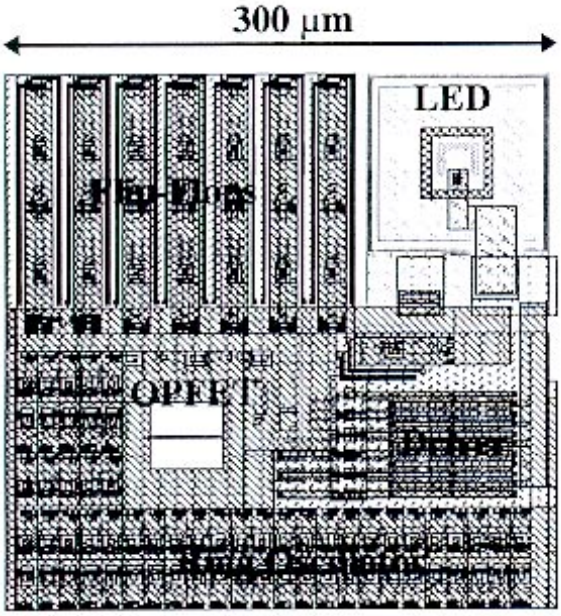


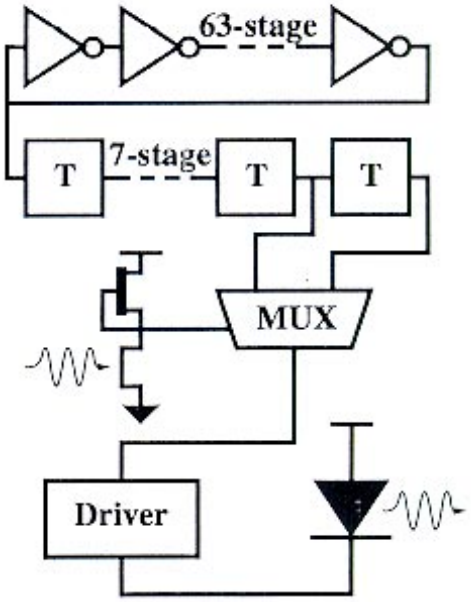
CIT:

- **4444 Pixels/cm^2**

Terabit Smart Pixel Arrays

1-Tbps/cm^2
= 1000 1-Gbps smart pixels in 1 cm^2

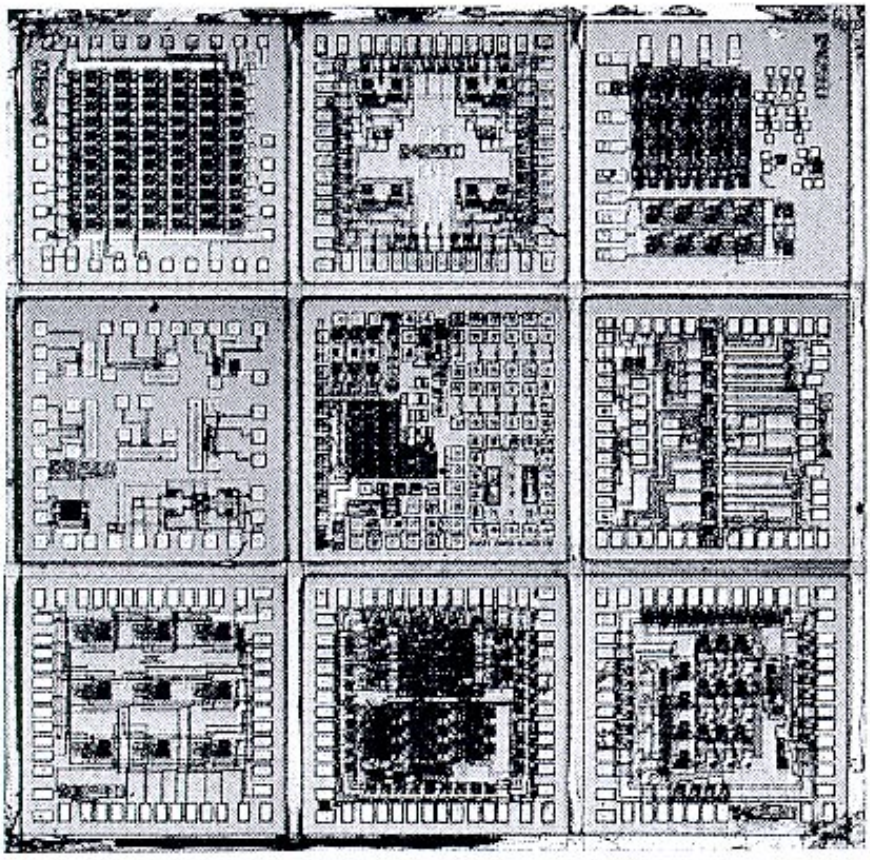




Power budget for 300x300 μm pixels:

Emitter:	5 mW
Detector:	5 mW
"smarts" ~ 40 Gates:	10 mW
Pixel Total:	20 mW
Power Density:	20 W/cm^2

True OE-VLSI



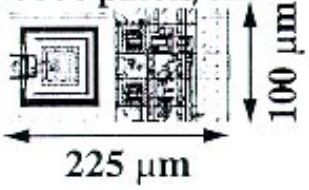
Standard Cells:

- LED
- Driver
- OPFET
- MSM

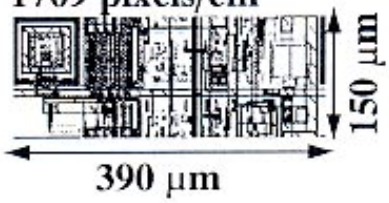
CAD Support:

- Synthesis
- Layout
- Extraction
- Verification

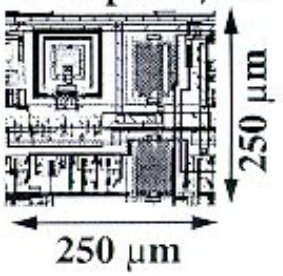
CIT:
4444 pixels/cm^2



USC:
1709 pixels/cm^2



CSU:
1600 pixels/cm^2



The OPTOCHIP Project: An OEIC foundry prototype

- **Participants** (first offering) -

"Optoelectronic Neural Array"
Jean-Jacques P. Drolet and Demetri Psaltis
California Institute of Technology, Pasadena, CA

"An OPTOCHIP for an Optoelectronic Connectionist Correlation Network"
Carl W. Wilmsen, Mahmood Azimi, Rick Snyder, and Eric Hayes
Colorado State University, Fort Collins, CO

"Integrated Source/Detector Array for Free-space Optical Interconnection Prototype Demonstration Systems"
Michael W. Haney, Marc P. Christensen, and Shaktish Acharya
George Mason University, Fairfax, VA

"Dynamic Smart Pixels for Photonic ATM Switch and Cross-bar"
Alain Shang, Pritham Sinha, and Frank Tooley
McGill University, Montreal, Canada

"Controller Interface for a Distributed Ensemble of Remote Sensors"
Lily Cheng, Edward Kolesar, and Stephen Weis
Texas Christian University, Fort Worth, TX

"Optoelectronic Error Diffusion Neural Network"
Barry L. Shoop, Eugene Ressler, Andre Sayles, James Loy, Gergory Tait, Daniel C. Gray, Bryan S. Goda, and James H. Wise
United States Military Academy, West Point, NY

"Optical Multi-channel Interconnection Network Interface using Monolithic Optoelectronic Integrated Circuits"
Timothy Pinkston
University of Southern California, Los Angeles, CA

"Smart Pixel Array Systems for Parallel Data Processing"
Alexander A. Sawchuk and Charles Kuznia

University of Southern California, Los Angeles, CA

"Multiplicative Lateral Inhibition Neural Networks (NLINN)"

W. Randall Babbit
University of Washington, Seattle, WA

OPTOCHIP SUMMARY

OPTOCHIP 1

Current status:

- Initial offering conducted Feb '96 to May '97
- Designs completed May '96
- Chips sent to groups for electrical test 9/11/96
- Completed OEICs sent to groups 5/2/97

Long term:

- Shorter wavelength LEDs: an option
- Resonant cavity LEDs: an option
- VCSELs: the more important objective

Beyond OPTOCHIP 1

We can offer a unique density and complexity of optoelectronic integration.

There is a user community eager...
...to have access to this technology, and
...to have VCSELS available in this technology.

The obvious conclusions are that...
...there should be more offerings,
...the technology should be extended,
(VCSELs, HGaAs4, 1.55 μm, etc.)

Epitaxy-on-Electronics Summary

ACCOMPLISHMENTS

1. Stability of GaAs ICs established and reduced temperature epitaxy techniques developed
    - upper temperature bound of 475˚C
    - atomic hydrogen oxide removal
    - InGaAsP as alternative to AlGaAs
2. Monolithic integration of heterostructure devices with MESFET VLSI electronics demonstrated
    - LEDs, SEEDs, RTDs
    - arbitrary device placement
    - unprecedented complexity
    - multi-gigahertz electronics
3. OEIC research foundry offered
    - user/designer/fabricator interfaces exercised
    - computer design tools available
    - robust technology developed

COMING ATTRACTIONS

1. VCSELs
    - major new campus effort initiated
2. Increased use of dry-etch techniques
    - new poly-strip process (CAIBE w. Cl_2, high T)
    - mirror etch for InGaP/GaAs mirrors, deflectors
3. HGaAs4 process
    - smaller size, higher speed

- excellent linear performance

4. New Vitesse msm process
    - improved high speed response
    - soon available through MOSIS

CONCLUDING REMARKS

* **Epitaxy on Electronics (EoE) is an important enabling technology...**

  ...for optoelectronic integration

  ...for integrating quantum effect and other heterostructure devices

* **Multi-project chips and projects like OPTOCHIP...**

  ...give many users access to the EoE technology

  ...generate need for, and stimulate development of, EoE and other integration technologies

****

"All major technological innovations have been important because of applications they created" **Herb Kroemer**

"I don't know all the many places we are going with OEICs, but we are definitely under way." **Clif Fonstad**

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